This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1-27. (Cancelled)

28. (Currently amended) A method of forming a semiconductor structure, the method comprising:

providing a strained semiconductor layer;

providing a SiGe layer over said strained semiconductor layer; and

selectively removing said SiGe layer to expose said strained semiconductor layer,

wherein selectively removing said SiGe layer comprises thermal oxidation performed at or below a temperature of approximately 850 °C.

29. (Previously presented) The method of claim 28, wherein said strained semiconductor layer comprises Si, Ge, or GaAs.

30. (Previously presented) The method of claim 28, further comprising, before the step of providing a strained semiconductor layer, providing a relaxed semiconductor layer beneath said strained semiconductor layer.

31. (Previously presented) The method of claim 30, wherein said relaxed semiconductor layer comprises Si or Ge.

32. (Previously presented) The method of claim 28, wherein said strained semiconductor layer is disposed over a semiconductor substrate.

33. (Previously presented) The method of claim 32, wherein said semiconductor substrate comprises Si.

34. (Previously presented) The method of claim 32 wherein said semiconductor substrate comprises an insulator layer.

35. (Previously presented) The method of claim 34, wherein said insulator layer comprises silicon dioxide.

36. – 37. (Cancelled)

38. (Currently amended) The method of claim [[36]]28, wherein said thermal oxidation is performed at a temperature at or below approximately 700°C.

39. (Previously presented) The method of claim 28, wherein said step of selectively removing said SiGe layer comprises chemical oxidation.

40. (Previously presented) The method of claim 28, wherein said step of selectively removing said SiGe layer is performed on a first region of said SiGe layer and not on a second region of said SiGe layer.

41. (Previously presented) The method of claim 40, wherein said method further comprises forming a MOSFET in said first region.

42. (Previously presented) The method of claim 41, wherein said MOSFET comprises a high-k dielectric.

43. (Previously presented) The method of claim 40, wherein said method further comprises forming a MOSFET in said second region.

44. (Previously presented) The method of claim 43, wherein said MOSFET comprises a high-k dielectric.

45. (Previously presented) The method of claim 40, wherein said method further comprises:

forming a surface channel device having a first channel in said first region; and

forming a buried channel device having a second channel in said second region,

wherein the strained semiconductor layer comprises said first channel and said second channel.

46. (Currently amended) A method of manufacturing a semiconductor device, comprising:

providing a strained semiconductor layer;

providing a SiGe layer over said strained semiconductor layer;

selectively removing said SiGe layer to expose said strained semiconductor layer;

providing a high-k gate dielectric over said strained semiconductor layer.

providing a source region in a first region of said strained semiconductor layer;

providing a drain region in a second region of said strained semiconductor layer; and

providing a gate contact disposed above said gate dielectric and between said source and drain regions.

47. (Previously presented) The method of claim 46, wherein said source region and said drain region are p-type doped.

48. (Previously presented) The structure of claim 46, wherein said source region and said drain region are n-type doped.

49. (Previously presented) The method of claim 46, wherein said strained semiconductor layer comprises Si, Ge, or GaAs.

50. (Previously presented) The method of claim 46, further comprising, before the step of providing a strained semiconductor layer, providing a relaxed semiconductor layer beneath said strained semiconductor layer.

51. (Previously presented) The method of claim 50, wherein said relaxed semiconductor layer comprises Si or Ge.

52. (Previously presented) The method of claim 46, wherein said strained semiconductor layer is disposed over a semiconductor substrate.

53. (Previously presented) The method of claim 52, wherein said semiconductor substrate comprises Si.

54. (Previously presented) The method of claim 52 wherein said semiconductor substrate comprises an insulator layer.

55. (Cancelled)

56. (New) A method of forming a semiconductor structure, the method comprising:
providing a strained semiconductor layer;
providing a SiGe layer over said strained semiconductor layer;
selectively removing said SiGe layer to expose said strained semiconductor layer in a first region but not in a second region; and
forming a MOSFET in the first region.

57. (New) The method of claim 56, wherein the MOSFET comprises a high-k dielectric.

58. (New) A method of forming a semiconductor structure, the method comprising:
providing a strained semiconductor layer;
providing a SiGe layer over said strained semiconductor layer;
selectively removing said SiGe layer to expose said strained semiconductor layer in a first region but not in a second region; and
forming a MOSFET in the second region.

59. (New) The method of claim 58, wherein the MOSFET comprises a high-k dielectric.

60. (New) A method of manufacturing a semiconductor device, comprising:

providing a strained semiconductor layer;

providing a SiGe layer over said strained semiconductor layer;

selectively removing said SiGe layer to expose said strained semiconductor layer;

providing a gate dielectric over said strained semiconductor layer.

providing a p-type-doped source region in a first region of said strained semiconductor layer;

providing a p-type-doped drain region in a second region of said strained semiconductor layer; and

providing a gate contact disposed above said gate dielectric and between said source and drain regions.

61. (New) The method of claim 60, wherein said strained semiconductor layer comprises Si, Ge, or GaAs.

62. (New) The method of claim 60, further comprising, before the step of providing a strained semiconductor layer, providing a relaxed semiconductor layer beneath said strained semiconductor layer.

63. (New) The method of claim 62, wherein said relaxed semiconductor layer comprises Si or Ge.

64. (New) The method of claim 60, wherein said strained semiconductor layer is disposed over a semiconductor substrate.

65. (New) The method of claim 64, wherein said semiconductor substrate comprises Si.

66. (New) The method of claim 64 wherein said semiconductor substrate comprises an insulator layer.

67. (New) A method of manufacturing a semiconductor device, comprising:

providing a strained semiconductor layer;

providing a SiGe layer over said strained semiconductor layer;

selectively removing said SiGe layer to expose said strained semiconductor layer;

providing a gate dielectric over said strained semiconductor layer.

providing an n-type-doped source region in a first region of said strained semiconductor layer;

providing an n-type-doped drain region in a second region of said strained semiconductor layer; and

providing a gate contact disposed above said gate dielectric and between said source and drain regions.

68. (New) The method of claim 67, wherein said strained semiconductor layer comprises Si, Ge, or GaAs.

69. (New) The method of claim 67, further comprising, before the step of providing a strained semiconductor layer, providing a relaxed semiconductor layer beneath said strained semiconductor layer.

70. (New) The method of claim 69, wherein said relaxed semiconductor layer comprises Si or Ge.

71. (New) The method of claim 67, wherein said strained semiconductor layer is disposed over a semiconductor substrate.

72. (New) The method of claim 71, wherein said semiconductor substrate comprises Si.

73. (New) The method of claim 71 wherein said semiconductor substrate comprises an insulator layer.